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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,844	09/12/2003	Joseph M. Jeddeloh	501321.01	7877

7590 04/11/2007

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2117	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,844	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-18 and 23-31* is/are allowed.

6)☒ Claim(s) *19-22 and 32-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered March 23, 2007.

- Claims 1-50 are pending.
- Claims 1-18 and 23-31 are allowed.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to claims 1-50 filed March 23, 2007 have been fully considered but they are moot under new grounds of rejection. Examiner acknowledges and wishes to express his thanks to Applicant's Representative Mr. Edward Bulchis for attempts to prosecute this Application as efficiently as possible. Since all claims are not allowable over prior art, Examiner is unable to amend claims 36, 42, 44 and 45 as discussed, because the emailed amendments are not considered official and are not part of the record. However, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 19-22 & 32-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. US Pat no. 6880117 B2 and further in view of Nadeau-Dostie et al.

As per claim 19:

Lin teaches a memory module, comprising: a memory device (Figure 2 # 50A-C); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 24); and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 24, column 4, lines 15-65)), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on

the received output signals whether the at least one memory device properly responded to the series of first signals.

Lin does not explicitly teach varying the frequency while the memory device is responding to a series of first signal and Lin does not teach testing a plurality of memory devices.

However, Nadeau-Dostie et al. in an analogous art teaches varying the frequency of the test clock while the digital device is responding to a series of first signals (Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Lin to test a plurality of memory devices and vary the frequency of the test clock, as that would enable Lin to test multiple memory devices in various time domains making the testing more efficient. Further, the frequency multiplier circuit in Lin possesses the ability to change the frequency of the test clock over a range, therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the multiplier circuit and vary the frequency in order to test how the memory devices respond to various frequencies.

As per claim 20:

Lin/Nadeau-Dostie et al. teach the memory module as rejected in claim 19 above, wherein the self-test module further comprises: a delay line receiving the clock signal from the variable frequency clock generator and generating a delayed internal clock signal (Nadeau-Dostie, Figure 4); and a flip-flop having a data input coupled to receive the first signal, a clock input coupled to receive the internal clock signal, and an output coupled to the at least one memory device (Figure 3).

As per claim 21:

Lin/Nadeau-Dostie teach the memory module as rejected in claim 19 above, wherein the memory hub further comprises an externally accessible maintenance port operable to provide access to signals indicative of whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 36).

As per claim 22:

Lin/Nadeau-Dostie teach the memory module as rejected in claim 19 above wherein the memory hub further comprises a plurality of link interfaces (Figure 2 # 40, 42, 44), a plurality of memory device interfaces (Figure 2 # 50A-C), and a switch for selectively coupling one of the plurality of link interfaces and one of the plurality of memory device interfaces (column 8, lines 5-60).

As per claims 32:

Lin substantially teaches a memory module, comprising: a memory device (Figure 2 # 50A-C); and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices (Figure 1 # 26); memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device (Figure 1 # 22); and a variable frequency clock generator producing and coupling to the at least one memory device a clock signal having a frequency corresponding to a frequency control signal (Figure 1 # 24);

and a self-test module coupled to at least one of the memory devices, the self-test module being operable to generate the frequency control signal so that the frequency of the clock signal varies over a range (Figure 1 # 24, column 4, lines 15-65)), the self-test module further being operable couple a series of first input signals to the at least one memory device and to receive output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first signals as the frequency of the clock signal is varied (Figure 1 # 34), at least one input device coupled to the peripheral device port of the system controller (Figure 1 # 32); at least one output device coupled to the peripheral device port of the system controller (Figure 1 # 38) and at least one data storage device coupled to the peripheral device port of the system controller (Figure 1 # 30).

Lin does not explicitly mention that processor having a processor bus or a system controlled having a system memory port, a peripheral device port and varying the frequency while the memory device is responding to a series of first signal and Lin does not teach testing a plurality of memory devices.

However, Nadeau-Dostie et al. in an analogous art teaches varying the frequency of the test clock while the digital device is responding to a series of first signals (Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable Lin to test a plurality of memory devices and vary the frequency of the test clock, as that would enable Lin to test multiple memory devices in various time domains making the testing more efficient.

Further, the frequency multiplier circuit in Lin possesses the ability to change the frequency of the test clock over a range, therefore it would be obvious to one of ordinary skill in the art at the time of the invention to use the multiplier circuit and vary the frequency in order to test how the memory devices respond to various frequencies. In addition, to realize that the apparatus taught in Lin generally includes standard equipment like a processor, processor bus, a controller, and various input/output ports. Therefore it would have been obvious to one with ordinary skill in the art at the time the invention was made to use the mentioned apparatus since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claims 33-35:

These claims are rejected under the same arguments as claims 20-22.

As per claim 36:

Lin/Nadeau-Dostie teach a method for performing signal timing testing on memory system having a memory hub coupled to a plurality of memory devices (Figure 1 # 26, Nadeau-Dostie, Abstract), the method comprising: generating testing signals in the memory hub (Figure 1 # 22); coupling the testing signals from the memory hub to the memory devices while varying the relative timing between when the testing signals are applied to the memory devices (Nadeau-Dostie, Abstract) generating output signals in the memory devices resulting from the testing signals; coupling the output signals from the memory devices to the memory hub; evaluating the output signals in the

memory hub to determine if the memory devices properly responded to the test signals (Figure 1 # 34).

As per claims 37-41:

Lin/Nadeau-Dostie teach the method as rejected in claim 36 above wherein the self-test module further comprises: a pattern generator producing a pattern of data bits each of which is used to generate a respective one the first signals in the series (Figure 1 # 32); and a comparator coupled to the pattern generator and to the at least one memory device, the comparator receiving output signals from the at least one memory device and determining a pattern of data corresponding thereto, the comparator further and comparing the pattern generated from the output signals to the pattern of data from which the first signals are generated (Figure 1 # 34), a storage device coupled to the comparator to store the results of the comparisons between the pattern generated from the output signals and the pattern of data from which the first signals are generated (Figure 1 # 30, column 5, lines 5-40).

As per claims 42-50:

Claims 42-50 are directed to a method of the system and memory modules of claims 19-22 & 32-41. Lin/Nadeau-Dostie teach, either alone or in combination as stated above, the system and memory modules as set forth in claims 19-22 & 32-41. Therefore, Lin/Nadea-Dostie also teach, either alone or in combination as stated above, the methods as set forth in claims 42-50.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance: The prior art of record does not teach the following limitations:

The present invention includes (claim 1) a memory module comprising: a plurality of memory devices; and a memory hub, comprising: a link interface for receiving memory requests for access to at least one of the memory devices; memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device; and a self-test module coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range, the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals.

Claim 11 teaches a memory module which includes capability to alter over a range the relative timing between when some of the first signals are used to latch the corresponding second signals.

Further claim 23 teaches a processor-based system, comprising: a processor having a processor bus; a system controller coupled to the processor bus, the system

controller having a system memory port and a peripheral device port; at least one input device coupled to the peripheral device port of the system controller; at least one output device coupled to the peripheral device port of the system controller; at least one data storage device coupled to the peripheral device port of the system controller; and a memory module coupled to the system memory port of the system controller, the memory module comprising: a plurality of memory devices; and a memory hub, comprising: a link interface coupled to the system memory port for receiving memory requests for access to at least one of the memory devices; a memory device interface coupled to the memory devices, the memory device interface coupling write memory requests and write data to the memory devices, the memory device interface further coupling read memory requests to the memory device and coupling read data from the memory device; and a self-test module coupled to at least one of the memory devices, the self-test module being operable to couple a series of corresponding first and second signals to the at least one memory device and to alter the relative timing between when some of the corresponding first and second signals in the series are coupled to the at least one memory device over a range, the self-test module further receiving output signals from the at least one memory device and determining based on the received output signals whether the at least one memory device properly responded to the series of first and second signals.

The prior arts of record Lin, US Pat no. 6,880,117 and Nadeau-Dostie US Pat no. 5,349,587 do not teach altering the relative timing between corresponding first and second test signals over a range, during the testing of a plurality of memory devices.

Claims 1, 11 and 23 alter the relative timing between corresponding first and second signals over a range during a specific test execution. However, prior arts of record teach altering relative timing of signals during different tests and not during a specific test execution.

For instance, Lin teaches testing a memory device while latching a plurality of testing signals using one two different clocks. However, the timing between two corresponding signals is not altered during a test execution over a range. Further, Nadeau-Dostie teaches a scan test of memory elements in different time domains but the relative timing between two corresponding test signals is not altered over a specific range.

Hence, the prior arts of record fail to anticipate or render obvious the claimed inventions. Thus claims 1-18 and 23-31 are allowable over the prior arts of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
04/05/2007

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